MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Digital Technologies**			**Module Delivery**	
Module Type	**Core**			☒ **Theory** ☒ **Lecture** ☒ **Lab** ☐ **Tutorial** ☒ **Practical** ☐ **Seminar**	
Module Code	**AIE125**				
ECTS Credits	**6**				
SWL (hr/sem)	**150**				
Module Level	1		**Semester of Delivery**	2	
Administering Department	Artificial intelligence		**College**	College of Engineering	
Module Leader	Abbas Abdulaali		**e-mail**	abbas.abdulali@alayen.edu.iq	
Module Leader's Acad. Title	Assistant Lecturer		**Module Leader's Qualification**	M.Sc.	
Module Tutor	Abbas Abdulaali		**e-mail**	abbas.abdulali@alayen.edu.iq	
Peer Reviewer Name	Name		**e-mail**	E-mail	
Scientific Committee Approval Date			**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

وزارة التعليم العالي والبحث العلمي
جامعة العين العراقية
كلية الهندسة
قسم الذكاء الاصطناعي

م.د. سرمد كاظم ذياب

Module Aims, Learning Outcomes and Indicative Contents

أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية

Module Objectives أهداف المادة الدراسية	1. Introduce the fundamental principles of digital systems and number systems. 2. Develop students' understanding of binary arithmetic and digital codes. 3. Study the operation and characteristics of basic logic gates. 4. Introduce Boolean algebra and its application in simplifying logic expressions. 5. Enable students to analyze and design combinational logic circuits. 6. Familiarize students with Karnaugh map techniques for logic minimization. 7. Train students to implement digital circuits using simulation tools such as Multisim.		
Module Learning Outcomes	Knowledge	A1	A1.1 **Define** the fundamental concepts of digital systems and distinguish between analog and digital quantities. A1.2 **Describe** number systems used in digital electronics including decimal, binary, octal, and hexadecimal systems. A1.3 **Explain** binary arithmetic operations and the representation of signed numbers using complement methods. A1.4 **Identify** the functions and characteristics of basic logic gates (NOT, AND, OR, NAND, NOR, XOR, XNOR).
		A2	A2.1 **Apply** Boolean algebra laws and rules to manipulate and simplify logic expressions. A2.2 **Interpret** truth tables and derive Boolean expressions for digital circuits.
		A4	A4.1 **Analyze** combinational logic circuits using Boolean expressions and truth tables. A4.2 **Design** combinational logic circuits such as adders, decoders, encoders, and comparators.
	Skills		

		B2	B2.1 Communicate effectively – graphically with a range of audiences using contemporary tools. B2.2 Communicate verbally and in writing with a range of audiences using contemporary tools.
	Ethics	C3	C3.1 Utilize contemporary technologies. C3.3Utilize health and safety requirements.

abbIndicative Contents

المحتويات الإرشادية

Part A – Digital Systems Fundamentals

1. Introduction to digital systems
2. Analog and digital quantities
3. Decimal number system

Part B – Number Systems and Codes

1. Binary number system
2. Decimal–binary conversions
3. Binary arithmetic
4. Signed numbers and complements
5. Octal and hexadecimal number systems
6. BCD and digital codes

Part C – Logic Gates

1. NOT gate
2. AND gate
3. OR gate
4. NAND gate
5. NOR gate
6. XOR and XNOR gates

Part D – Boolean Algebra

1. Boolean operations and expressions
2. Laws and rules of Boolean algebra
3. DeMorgan's theorem
4. Simplification using Boolean algebra

Part E – Logic Minimization

1. Truth tables

	2. Standard forms of Boolean expressions 3. Karnaugh map minimization 4. SOP and POS simplification **Part F – Combinational Logic Circuits** 1. Universal gates (NAND and NOR) 2. Binary adders 3. Comparators 4. Decoders and encoders 5. Code converters 6. Multiplexers and demultiplexers 7. Parity generators and checkers

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	• Presentation • Interactive learning • Discussions • Brainstorming • Group Solving Problems • Problem-Based Learning • Self-learning

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	65	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	5
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	85	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	6
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**150**		

Module Evaluation

تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
SFormative assessment	Quizzes	2	10% (10)	5 and 10	A1.1, A1.2, A1.3, A1.4, A2.1, A2.2, A4.1
	Assignments	2	10% (10)	2 and 12	A2.1, A2.2, A4.1, A4.2, B2.1, B2.2
	Projects / Lab.	1	10% (10)	Continuous	A4.1, A4.2, B2.1, B2.2, C3.1, C3.3
	Report	1	10% (10)	13	B2.2, C3.1
Summative assessment	Midterm Exam	2hr	10% (10)	7	A1.1, A1.2, A1.3, A1.4, A2.1
	Final Exam	3hr	50% (50)	16	A1.1, A1.2, A1.3, A1.4, A2.1, A2.2, A4.1, A4.2
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)

المنهاج الاسبوعي النظري

	Material Covered	Los
Week 1	Introduction to Digital Systems, Analog vs Digital Quantities, Decimal Numbers	A1.1
Week 2	Binary Numbers, Conversions, Binary Arithmetic	A1.3
Week 3	1's and 2's Complement of Binary Numbers, Signed Numbers and their Arithmetic Operations	A1.3
Week 4	Hexadecimal and Octal Numbers, BCD Codes	A1.2
Week 5	The Inverter, The AND Gate, The OR Gate, The NAND Gate, The NOR Gate, The Exclusive-OR and Exclusive-NOR Gates.	A1.4, B2.1
Week 6	Boolean Operations and Expressions, Laws and Rules of Boolean Algebra, DeMorgan's Theorem, Simplification using Boolean Algebra	A2.1
Week 7	Mid-term Exam + Standard Forms of Boolean Expressions.	A2.1
Week 8	Boolean Expressions and Truth Tables.	A2.2, B2.1
Week 9	The Karnaugh Map, Karnaugh Map SOP Minimization.	A4.1, B2.1
Week 10	Karnaugh Map POS Minimization.	A4.1
Week 11	Basic Combinational Logic Circuits and their implementation, Universal Properties of NAND and NOR Gates, and their use in Combinational Logic, Logic Circuit Operation with pulse Waveforms.	A4.1, C3.1
Week 12	Basic and Parallel Binary Adders.	A4.2, B2.2

Week 13	Comparators, Decoder.	A4.2
Week 14	Encoder, Code Converters.	A4.2, C3.3
Week 15	Multiplexers, Demultiplexers, Parity Generators/Checkers.	A4.2
Week 16	Preparatory week before the final Exam.	All

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر		
	Material Covered	**Los**
Week 1-3	Logic Gates	B2.1, C3.3
Week 4-6	Combinational Logic Circuits	B2.1, C3.1
Week 7-9	Karnaugh Maps	B2.1, A4.1
Week 10-11	Code Conversion	B2.1, B2.2
Week 12-13	Basic Arithmetic Operations	B2.2, A4.2
Week 14-15	Comparators	B2.1, C3.1, C3.3

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	M. Morris Mano & Michael D. Ciletti **Digital Design**, 5th Edition, Pearson Education, 2013. Thomas L. Floyd **Digital Fundamentals**, 11th Edition, Pearson Education, 2015.	Yes
Recommended Texts	Stephen Brown & Zvonko Vranesic **Fundamentals of Digital Logic with Verilog Design**, 3rd Edition, McGraw-Hill, 2013. Ronald J. Tocci, Neal Widmer & Gregory Moss **Digital Systems: Principles and Applications**, 12th Edition, Pearson, 2017. Charles H. Roth Jr. & Larry L. Kinney **Fundamentals of Logic Design**, 7th Edition, Cengage Learning, 2014.	No
Websites	https://eng.alayen.edu.iq/colleges/e/42	

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks %**	**Definition**
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.